

### Evaluation Scheme of M. Tech Embedded System Design

FIRST SEMESTER								
Course code	Course title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	EXTENAL	INTERNAL	TOTAL
MTED 101	Digital Systems Design	3	1	0	4	100	50	150
MTED 102	Data Communication & Networks	3	1	0	4	100	50	150
MTED 103	Designing with Power Devices	3	1	0	4	100	50	150
MTED 104	Real Time Systems	3	1	0	4	100	50	150
MTED 105	Software Technology for Embedded Systems	3	1	0	4	100	50	150
MTED 106	Software Technology-lab	0	0	4	4	50	50	100
MTED 107	Digital Design and Implementation LAB	0	0	4	4	50	50	100
Grand total		15	5	8	28	700	350	1050
SECOND SEMESTER								
Course code	Course Title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	INTERNAL	EXTERNAL	TOTAL
MTED 201	Embedded System Design	3	1	0	4	50	100	150
MTED 202	Neural Networks & Fuzzy Logic	3	1	0	4	50	100	150
MTED 203	Advanced Micro processor and micro controllers	3	1	0	4	50	100	150
MTED 204	Real Time Operating System	3	1	0	4	50	100	150
MTED 205	Computer Architecture	3	1	0	4	50	100	150
MTED 206	Advanced Micro Controller-LAB	0	0	4	4	50	100	100
MTED 207	Real Time Operating System -LAB	0	0	4	4	50	100	100
Grand total		15	5	8	28	350	700	1050
THIRD SEMESTER								
Course code	Course title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	INTENAL	EXTERNAL	TOTAL
MTED 301	Electronic Instrumentation Technology	3	1	0	4	50	100	150
MTED 302	System On Chip	3	1	0	4	50	100	150
MTED 303	RF Design	3	1	0	4	50	50	150
MTED 304	Thesis Seminar*	0	0	10	10	50	100	150
Grand total		6	2	10	18	150	300	600
FOURTH SEMESTER								
Course Code	Subject	Schedule of Teaching						
		L	T	P	TOTAL			
MTED 401	THESIS*	0	0	28	28			

\*The students will complete their Thesis work and submit copies of the Thesis report to the University as per its existing procedures. The Internal and External Examiners appointed by the University will evaluate the same through a Viva-voce examination and award Distinction / Pass / Fail to the Thesis.

### Evaluation Scheme of M. Tech VLSI Design

FIRST SEMESTER								
Course code	Course title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	Theory/ Practical	Sessional	TOTAL
VL-511	Semiconductor Devices	3	1	0	4	50	50	100
VL-512	VLSI Design concepts	3	1	0	4	50	50	100
VL-513	Hardware Description Languages	3	1	0	4	50	50	100
VL-514	VLSI Technology	3	1	0	4	50	50	100
VL-515	Design of Analog/Mixed Mode VLSI Circuits	3	1	0	4	50	50	100
VL-516	VLSI Design-LAB	0	0	4	4	50	50	100
VL-517	Hardware Description Language -LAB	0	0	4	4	50	50	100
Grand total		15	5	8	28	350	350	700
SECOND SEMESTER								
Course code	Course title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	Theory/ Practical	Sessional	TOTAL
VL-521	Advanced Digital Signal Processing	3	1	0	4	50	50	100
VL-522	ASIC Design and FPGA	3	1	0	4	50	50	100
VL-523	Memory Design and Testing	3	1	0	4	50	50	100
VL-524	Embedded Systems	3	1	0	4	50	50	100
VL-525	Testing and Fault Tolerance	3	1	0	4	50	50	100
VL-526	Digital Signal Processing and Embedded Systems- LAB	0	0	4	4	50	50	100
VL-527	Designing with FPGA's – LAB	0	0	4	4	50	50	100
Grand total		15	5	8	28	350	350	700
THIRD SEMESTER								
Course code	Course title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	Theory/ Practical	Sessional	TOTAL
VL-531	Elective-I	3	1	0	4	50	50	100
VL-532	Elective-II	3	1	0	4	50	50	100
VL-533	Thesis Seminar*	0	0	20	20	100	100	200
Grand total		6	2	20	28	200	200	400
LIST OF ELECTIVES								
Course code	Course title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	Theory/ Practical	Sessional	TOTAL
VL-E1	System on Chip (SOC)	3	1	0	4	50	50	100
VL-E2	RF Design	3	1	0	4	50	50	100
VL-E3	Process and Device Characterization and Measurements	0	1	0	4	50	50	100
VL-E4	Sensor Technology and MEMS	3	1	0	4	50	50	100
FOURTH SEMESTER								
Course code	Subject	Schedule of Teaching				Marks Distribution		
		L	T	p	TOTAL	Theory/ Practical	Sessional	TOTAL
VL-541	Thesis*	0	0	28	28	-	-	-

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## Evaluation Scheme of Electronics Product Design and Technology

FIRST SEMESTER								
Course code	Course title	Load Allocation				Marks Distribution		
		L	T	P	TOTAL	Theory/ Practical	Sessional	TOTAL
MTET 101	Microelectronics Technology	3	1	0	4	100	50	150
MTET 102	Computer Integrated Manufacturing Systems	3	1	0	4	100	50	150
MTET 103	Advanced Communication Systems	3	1	0	4	100	50	150
MTET 104	Advanced Digital System Design	3	1	0	4	100	50	150
MTET 105	Designing with Power Devices	3	1	0	4	100	50	150
MTET 106	CAD/CAM LAB	0	0	4	4	100	50	150
MTET 107	Advanced Digital Design and Implementation – LAB	0	0	4	4	100	50	150
Grand total		15	5	8	28	700	350	1050
SECOND SEMESTER								
Course code	Course Title	Load Allocation				Marks Distribution		
		L	T	P	TOTAL	EXTENAL	INTERNAL	TOTAL
MTET 201	Embedded System Design	3	1	0	4	100	50	150
MTET 202	Neural Networks & Fuzzy Logic	3	1	0	4	100	50	150
MTET203	Advanced Digital Signal Processing	3	1	0	4	100	50	150
MTET 204	Physical design of Electronic Equipments	3	1	0	4	100	50	150
MTET 205	Advanced Micro Controllers	3	1	0	4	100	50	150
MTET 206	Advanced Micro Controller-LAB	0	0	4	4	50	50	100
MTET 207	Digital Signal Processing LAB	0	0	4	4	50	50	100
Grand total		15	5	8	28	700	350	1050
THIRD SEMESTER								
Course code	Course Title	Load Allocation				Marks Distribution		
		L	T	p	TOTAL	EXTENAL	INTERNAL	TOTAL
MTED 301	Electronic Instrumentation Technology	3	1	0	4	100	50	150
MTED 302	System On Chip	3	1	0	4	100	50	150
MTET 301	Sensor Technology and MEMS	3	1	0	4	50	50	150
MTED 304	Thesis Seminar*	0	10	10	10	100	50	150
Grand total		6	2	10	18	300	150	600
FOURTH SEMESTER								
SUBJECT CODE	SUBJECT	SCHEDULE OF TEACHING						
		L	T	P	TOTAL			
MTET 401	Thesis*	0	0	28	28			

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