TIME TABLE

SEMESTER-I

VLSI DESIGN						
	9.00-10.00	10.00-11.00	11.30-12.30	12.30-1.30	1.30-2.30	2.30-4.00
Monday	VDC(41)	HDL(41)	VT (41)	RM(41)		VDC Lab(40A)
Tuesday	HDL(41)	DAM(40A)	VT (41)	VDC(41)		HDL Lab(40A)
Wednesday	VT(41)	HDL(41)	DAM(41)	RM(41)	LUNCH	VDC Lab(40A)
Thursday	DAM(41)	HDL(41)	VDC(41)	DCS		HDL Lab(40A)
Friday	VT(41)	VDC(41)	DAM(41)	RM(41)		

ELECTRONIC PRODUCT DESIGN & TECHNOLOGY (EPDT)						
	9.00-10.00	10.00-11.00	11.30-12.30	12.30-1.30	1.30-2.30	2.30-4.00
Monday	MP(40A)	ADSD(41)	EPD(40)	RM(41)		MP Lab(41A)
Tuesday	ADSD(41)	DPD(41)	MP(40A)	EPD(10)		ADSD Lab(40)
Wednesday	DPD(40)	ADSD(41)	EPD(10)	RM(41)	LUNCH	MP Lab(41A)
Thursday	MP(40A)	ADSD(41)	DCS	DPD()41		ADSD Lab(40)
Friday	DPD(40)	MP(40A)	EPD(10)	RM(41)		

EMBEDDED SYSTEMS (ES)						
	9.00-10.00	10.00-11.00	11.30-12.30	12.30-1.30	1.30-2.30	2.30-4.00
Monday	DCN(41A)	DSD(41)	ST(10)	RM(41)		ST Lab(41A)
Tuesday	DSD(41)	DPD(41)	DCN(41A)	ST(41A)		DSD Lab(40)
Wednesday	DPD(40)	DSD(41)	DCN(41A)	RM(41)	LUNCH	ST Lab(41A)
Thursday	ST(10)	DSD(41)	DCN(41A)	DPD(41)		DSD Lab(40)
Friday	DPD(40)	DCN(41A)	DCS	RM(41)		
* DCS --- Doubt Clearance Session						