



## Study Scheme 2018 for M.Tech. VLSI Design

### Semester-1

Sem	Course Code	Course Name	L	T	P	Hrs	Internal	External	Total	Credits
1	MTVL-101-18	CMOS VLSI Design	3	0	0	3	40	60	100	3
1	MTVL-102-18	RTL Simulation & Synthesis with PLD	3	0	0	3	40	60	100	3
1	MTVL-PE1X-18	Program Elective – 1	3	0	0	3	40	60	100	3
1	MTVL-PE2Y-18	Program Elective – 2	3	0	0	3	40	60	100	3
1	MTVL-111-18	VLSI Design Concepts LAB	0	0	4	4	60	40	100	2
1	MTVL-112-18	RTL Simulation & Synthesis with PLD LAB	0	0	4	4	60	40	100	2
1	MTRM-101-18	Research Methodology and IPR	2	0	0	2	40	60	100	2
1	MTAU-AXX-18	Audit Course 1	0	0	0	0	40	60	100	0
		<b>Total</b>	<b>14</b>	<b>0</b>	<b>8</b>	<b>22</b>	<b>360</b>	<b>440</b>	<b>800</b>	<b>18</b>

### Semester-2

Sem	Course Code	Course Name	L	T	P	Hrs	Internal	External	Total	Credits
2	MTVL-103-18	Analog, Digital & Mixed Signal CMOS Design	3	0	0	3	40	60	100	3
2	MTVL-104-18	VLSI Design Verification & Testing	3	0	0	3	40	60	100	3
2	MTVL-PE3X-18	Program Elective – 3	3	0	0	3	40	60	100	3
2	MTVL-PE4Y-18	Program Elective – 4	3	0	0	3	40	60	100	3
2	MTVL-113-18	Analog, Digital & Mixed Signal CMOS Design LAB	0	0	4	4	60	40	100	2
2	MTVL-114-18	VLSI Design Verification & Testing LAB	0	0	4	4	60	40	100	2
2	MTVL-MP1-18	Mini Project	0	0	4	4	60	40	100	2
2	MTAC-AYY-18	Audit Course 2	0	0	0	0	40	60	100	0
		<b>Total</b>	<b>12</b>	<b>0</b>	<b>12</b>	<b>24</b>	<b>380</b>	<b>420</b>	<b>800</b>	<b>18</b>



**Semester-3**

Sem	Course Code	Course Name	L	T	P	Hrs	Internal	External	Total	Credits
3	<b>MTVL-PE5X-18</b>	Program Elective-V	3	0	0	3	40	60	100	3
3	<b>MTOE-301X-18</b>	Open Elective	3	0	0	3	40	60	100	3
3	<b>MTAC-DS1-18</b>	Dissertation Phase-I	0	0	20	20	60	40	100	10
		<b>Total</b>	<b>6</b>	<b>0</b>	<b>20</b>	<b>26</b>	<b>140</b>	<b>160</b>	<b>300</b>	<b>16</b>

**Semester-4**

Sem	Course Code	Course Name	L	T	P	Hrs	Internal	External	Total	Credits
4	<b>MTVL-DS2-18</b>	Dissertation Phase-II	6	0	20	20	60	40	100	16
		<b>Total</b>				<b>68</b>	<b>960</b>	<b>1060</b>	<b>2000</b>	<b>68</b>

**PROGRAMME ELECTIVE COURSES**

	<b>Programme Elective-I</b>
<b>MTVL-PE1A-18</b>	CAD of Digital System
<b>MTVL-PE1B-18</b>	Advanced Digital Signal Processing
<b>MTVL-PE1C-18</b>	VLSI Interconnects
	<b>Programme Elective-II</b>
<b>MTVL-PE2A-18</b>	VLSI Technology
<b>MTVL-PE2B-18</b>	Memory Design and Testing
<b>MTVL-PE2C-18</b>	Embedded System Design
	<b>Programme Elective-III</b>
<b>MTVL-PE3A-18</b>	Low Power VLSI Design
<b>MTVL-PE3B-18</b>	Modeling and Simulation
<b>MTVL-PE3C-18</b>	Nano Materials & Nano Technology
	<b>Programme Elective-IV</b>
<b>MTVL-PE4A-18</b>	Semiconductor Devices
<b>MTVL-PE4B-18</b>	Parallel Processing
<b>MTVL-PE4C-18</b>	System on Chip (SOC)
	<b>Programme Elective-V</b>
<b>MTVL-PE5A-18</b>	Sensor Technology and MEMS
<b>MTVL-PE5B-18</b>	Process and Device Characterization & Measurements
<b>MTVL-PE5C-18</b>	RF Circuit Design



# FIRST SEMESTER

M.Tech (VLSI Design)



MTVL-101-18	Credits	L	T	P	Int	Ext
<b>CMOS VLSI Design</b>	3	3	0	0	40	60

## Course Objective

This is one of the fundamental courses meant to give basic insight into CMOS technology and understand the concepts & behavior and working of CMOS circuits for better VLSI system design.

## Course Outcomes

At the end of the course, students will be able to:

1. Understand the significance MOS technology in IC industry
2. Familiarity of CMOS circuit design and performance issues
3. Understand different logic techniques for high performance and low power IC applications

## Unit 1: Introduction to MOS Circuits

MOS Transistor Theory - Introduction MOS Device Design Equations, MOS Transistor as a Switches, Pass Transistor, CMOS Transmission Gate, Complementary CMOS Inverter, Static Load MOS Inverters, Inverters with NMOS loads, Differential Inverter, Tri State Inverter, BiCMOS Inverter.

## Unit 2: Circuit Characterization and Performance Estimation

Delay Estimation, Logical Effort and Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, Design Margin and Reliability.

## Unit 3: CMOS Circuit and Logic Design

CMOS Logic Gate Design, Physical Design of CMOS Gate, Designing with Transmission Gates, CMOS Logic Structures, Clocking Strategies, I/O Structures.

## Unit 4: CMOS Sub System Design

Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Zero/One Detectors, Binary Counters, ALUs, Multipliers, Shifters, Memory Elements, Control- FSM, Control Logic Implementation.

## Unit 5: Low Power CMOS VLSI Design

Introduction to Low Power Design, Power Dissipation in FET Devices, Power Dissipation in CMOS, Low-Power Design through Voltage Scaling – VT CMOS Circuits, MTCMOS Circuits, Architectural Level Approach – Pipelining and Parallel Processing Approaches, Low Power Basics CMOS Gate and Adder Design.

## Recommended Books

1. Sung Ms Kang, and Yusuf Lablebici, *CMOS Digital Integrated Circuits: Analysis & Design*, Tata McGraw-Hill Education
2. N. Weste and K. Eshraghian, *Principles of CMOS VLSI Design*, Addison Wesley
3. Neil H.E. Weste, David Harris, and Ayan Banerjee, *CMOS VLSI Design: A Circuits and Systems Perspective*
4. Kiat-Seng Yeo, Kaushik Roy, Low-Voltage, *Low-Power VLSI Subsystems*, McGraw-Hill Professional
5. Gary K. Yeap, *Practical Low Power Digital VLSI Design*, Kluwer Academic Press
6. Jan M. Rabaey, *Digital Integrated Circuits: A Design Perspective*, Pearson Education
7. Jacob Backer, Harry W. Li and David E. Boyce, *CMOS Circuit Design, Layout and Simulation*, Prentice Hall of India



MTVL-102-18	Credits	L	T	P	Int	Ext
RTL Simulation & Synthesis with PLD	3	3	0	0	40	60

## Course Objective

This is basic course meant to give hands on experience of various EDA tools for digital system design at RTL level simulation and implementation with different programmable devices available in semiconductor industry.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Familiarity of Finite State Machines, RTL design using reconfigurable logic.
2. Design and develop IP cores and Prototypes with performance guarantees
3. Use EDA tools like Cadence, Mentor Graphics and Xilinx.

## Unit 1: Design Approaches

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static Timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

## Unit 2: Basics of VHDL and Verilog HDL

Design entry by VHDL, Features of VHDL, Capabilities, Syntax and Semantics of VHDL; Basic Language Elements- Data objects Operators and signal assignments, Design Suits. Introduction to Verilog, Need of FSM, digital circuit design using FSM.

## Unit 3: Programmable Devices

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA elements- basic blocks, Programming Technologies- OTP, reprogrammable, I/O blocks, Programmable interconnects, Software, SoC, ESD protection.

## Unit 4: Design Techniques

Design for performance, Low power VLSI design techniques. Design for testability techniques- Ad-hoc, Partial and full scan techniques, BIST.

## Unit 5: IP and Prototyping

IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping

## Unit 6: Case Studies

Case studies and Speed issues.

## Recommended Books

1. Richard S. Sandige, *Modern Digital Design*, MGH, International Editions
2. Donald D Givone, *Digital Principles and Design*, TMH
3. Charles Roth, Jr. and Lizy K John, *Digital System Design using VHDL*, Cengage Learning.
4. Samir Palnitkar, *Verilog HDL, A Guide to Digital Design and Synthesis*, Prentice Hall.
5. Doug Amos, Austin Lesea, Rene Richter, *FPGA based prototyping Methodology Manual*, Xilinx
6. Bob Zeidman, *Designing with FPGAs & CPLDs*, CMP Books



MTVL-PE1A-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 1CAD of Digital System</b>	3	3	0	0	40	60

## Course Objective

This is course deals with Digital VLSI system design, testing and verification using different latest CAD tools and make students readily trained for career in VLSI industry.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Fundamentals of CAD tools for modeling, design, test and verification of VLSI systems.
2. Study of various phases of CAD, including simulation, physical design, test and verification.
3. Demonstrate knowledge of computational algorithms and tools for CAD.

## Unit 1: Introduction to VLSI Methodologies

Design flow, New trends in VLSI, Design Styles-full custom, standard cell, gate array, FPGA, Fabrication of VLSI Devices.

## Unit 2: VLSI design automation tools

Data structures and basic algorithms, graph theory and Computational complexity, tractable and intractable problems.

## Unit 3: General purpose methods for combinational optimization

Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms.

## Unit 4: Placement, floor planning & pin assignment

Problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment.

## Unit 5: Global Routing

Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches.

## Unit 6: Detailed routing

Problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms. VHDL/Verilog based implementation of simple digital Combinational and Sequential circuits.

## Recommended Books

1. N.A. Sherwani, *Algorithms for VLSI Physical Design Automation*.
2. S.H. Gerez,, *Algorithms for VLSI Design Automation*.
3. ChristophnMeinel& Thorsten Theobold, *Algorithm and Data Structures for VLSI Design*, KAP.



MTVL-PE1B-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 1</b> <b>Advanced Digital Signal Processing</b>	3	3	0	0	40	60

## Course Objective

This course deals with fundamental concepts of digital signal processing at system level and provides skills in developing application oriented algorithms and implementation intricacies in advanced DSP processors.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. To understand theory of different filters and algorithms
2. To understand theory of multirate DSP, solve numerical problems and write algorithms
3. To understand theory of prediction and solution of normal equations
4. To know applications of DSP at block level.

## Unit 1: Overview of DSP

Overview of DSP, Characterization in time and frequency, FFT Algorithms, Digital filter design and structures: Basic FIR/IIR filter design & structures, design techniques of linear phase FIR filters, IIR filters by impulse invariance, bilinear transformation, FIR/IIR Cascaded lattice structures, parallel realization of IIR.

## Unit 2: Multi rate DSP

Multi rate DSP, Decimators and Interpolators, Sampling rate conversion, multistage decimator & interpolator, poly phase filters, QMF, digital filter banks, Applications in subband coding.

## Unit 3: Filters

Linear prediction & optimum linear filters, stationary random process, forward-backward linear prediction filters, solution of normal equations, AR Lattice and ARMA Lattice-Ladder Filters, Wiener Filters for Filtering and Prediction.

## Unit 4: Algorithms

Adaptive Filters, Applications, Gradient Adaptive Lattice, Minimum mean square criterion, LMS algorithm, Recursive Least Square algorithm

## Unit 5: Nonparametric and Parametric Methods

Estimation of Spectra from Finite-Duration Observations of signals, Nonparametric Methods for Power Spectrum Estimation, Parametric Methods for Power Spectrum Estimation, Minimum-Variance Spectral Estimation, Eigen analysis Algorithms for Spectrum Estimation.

## Unit 6: Applications of DSP

Application of DSP & Multi rate DSP, Application to Radar, introduction to wavelets, application to image processing, design of phase shifters, DSP in speech processing & other applications

## Recommended Books

1. J. G. Proakis and D. G. Manolakis, *Digital signal processing: Principles, Algorithm and Applications*, 4<sup>th</sup> Edition, Prentice Hall.
2. N. J. Fliege, *Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets*, 1<sup>st</sup> Edition, John Wiley and Sons Ltd.
3. Bruce W. Suter, *Multirate and Wavelet Signal Processing*, 1<sup>st</sup> Edition, Academic Press.
4. M. H. Hayes, *Statistical Digital Signal Processing and Modeling*, John Wiley & Sons Inc...
5. S. Haykin, *Adaptive Filter Theory*, 4<sup>th</sup> Edition, Prentice Hall.
6. D. G. Manolakis, V.K. Ingle and S.M.Kogon, *Statistical and Adaptive Signal Processing*, McGraw Hill.

MTVL-PE1C-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 1</b> <b>VLSI Interconnects</b>	3	3	0	0	40	60

## Course Objective

This course provides basic knowledge about signaling issues that need be considered in system level VLSI design to suit high performance and low power applications.

## Course Outcomes

At the end of this course, students will be able

- To understand theory of different metals used for routing in ICs
- To understand scaling issues in Interconnects and their impact on overall IC performance
- Familiarity with various interconnect strategies for high speed and low power, low noise applications

## Unit 1: Interconnect Parameters

Resistance, Inductance, and Capacitance, Interconnect RC Delays: Elmore Delay Calculation. Interconnect Models: The lumped RC Model, the distributed RC Model, the transmission line model. SPICE Wire Models: Distributed RC lines in SPICE, Transmission line models in SPICE.

## Unit 2: Scaling issues in interconnects

Gate and Interconnect Delay, CMOS Repeater: The Static Behavior- Switching Threshold, Noise Margins, The Dynamic Behavior- Computing the capacitances, Propagation Delay: First order Analysis, Propagation Delay from a Design perspective, Power, energy and Energy-Delay- Dynamic Power Consumption, Static Consumption, Analyzing Power Consumption using SPICE

## Unit 3: Repeater Design

Driving Interconnects for Optimum speed and power Short channel model of CMOS Repeater - Transient Analysis of an RC loaded CMOS repeater, Delay Analysis, Analytical power expressions: Dynamic power, Short circuit Power, Resistive Power Dissipation, CMOS Repeater insertion: Analytical expressions for delay and power of a repeater chain driving an RC load.

## Unit 4: Advanced Interconnect Techniques

Reduced-swing Circuits, Current-mode Transmission Techniques.





## Unit 5: Crosstalk

Theoretical basis and circuit level modeling of crosstalk, Energy dissipation due to crosstalk: Model for energy calculation of two coupled lines. Contribution of driver and interconnect to dissipated energy, Crosstalk effects in logic VLSI circuits: Static circuits, Dynamic circuits and various remedies.

## Recommended Books

1. John P. Uymera, *Introduction to VLSI Circuits and Systems*, Wiley Student Edition.
2. S.M. Kang, L. Yusuf, *CMOS Digital Integrated Circuits-Analysis and Design TMH*, 3rd Edition.
3. Jan M. Rabaey, *Analysis and Design of Digital Integrated Circuits– A design Perspective*, TMH, 2nd Edition 2003.
4. F. Moll, M. Roca, *Interconnection Noise in VLSI Circuits*, Kluwer Academic Publishers

MTVL-PE2A-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 2</b> <b>VLSI Technology</b>	3	3	0	0	40	60

## Course Objective

.This course gives insight into VLSI industry fabrication process from Silicon to IC.

## Course Outcomes

At the end of this course, students will be able to:

1. Get exposure to detailed VLSI fabrication steps followed in fab houses
2. Understand the clean room concept and safety measurements followed at fabrication time.
3. Understand various techniques and methods use in ULSI fabrication: from raw material to IC

## Unit 1: Environment for VLSI Technology

Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

## Unit 2: Impurity incorporation

Solid State diffusion modeling and technology; Ion Implantation modeling, technology and damage annealing; characterization of Impurity profiles.

## Unit 3: Oxidation

Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation Technologies in VLSI and ULSI; Characterization of oxide films; High k and low k dielectrics for ULSI.

## Unit 4: Lithography

Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

## Unit 5: Chemical Vapour Deposition techniques

CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modeling and technology.



## Unit 6: Metal film deposition

Evaporation and sputtering techniques. Failure mechanisms in metal Interconnects; Multi-level metallization schemes

## Unit 7: Plasma and Rapid Thermal Processing

PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology

## Recommended Books

1. S. M. Sze (Ed), *VLSI Technology*, 2nd Edition, McGraw-Hill.
2. C.Y. Chang and S.M. Sze (Ed), *ULSI Technology*, McGraw-Hill Companies Inc.
3. S. K. Gandhi, *VLSI fabrication Principles*, John Wiley Inc.
4. B.Raj& Singh ,*VLSI Fabrication Technology* , Laxmi Publications
5. Sorab K. Gandhi, *The Theory and Practice of Microelectronics*, John Wiley & Son.
6. B.G Streetman, *VLSI Technology*, Prentice Hall.
7. A.S Grove, *Physics and Technology of semiconductor devices*, John Wiley & Sons

MTVL-PE2B-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 2</b>						
<b>Memory Design and Testing</b>	3	3	0	0	40	60

## Course Objective

This is course deals with fundamental designing concepts of various memory technologies, techniques and architectures and algorithms for modeling and testing the designed RAMs

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. understand different memory technologies
2. understand theory for designing of different memory architectures and issues related
3. understand theory for the testing of designed memories and explore different algorithm level fault modelling

## Unit 1: Random Access Memory Technologies

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies Application Specific SRAMs.

## Unit 2: Dynamic Random Access Memories (DRAMs)

DRAM Technology Development-CMOS DRAMs DRAMs Cell Theory and Advanced Cell Structures - BiCMOS DRAMs-Soft Error Failures in DRAMs Advanced DRAM Designs and Architecture-Application Specific DRAMs.

## Unit 3: Nonvolatile Memories

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read Only Memories (PROMs)-Bipolar PROMs-CMOS PROMs-Erasable (UV) -Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture..



## Unit 4: Memory Fault Modeling

Testing, And Memory Design For Testability And Fault Tolerance RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. Semiconductor Memory Reliability and Radiation Effects.

### Recommended Books

1. A.K Sharma, *Semiconductor Memories Technology, Testing and Reliability*, illustrated Edition, IEEE Press.
2. Gerald Luecke, Jack P. Mize, William N. Carr, *Semiconductor Memory design & application*, illustrated Edition, Mc-Graw Hill.
3. *Memory Technology design and testing*, IEEE International Workshop on: IEEE Computer Society Sponsor (S).
4. Parag K. Lala, *An Introduction to Logic Circuit Testing*, Morgan & Claypool Publishers.
5. Viswani D. Agarwal Michael L. Bushnell, *Essentials of Electronic Testing for Digital Memory & Mixed Signal VLSI Circuit*, Kluwer Academic Publications.

MTVL-PE2C-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 2 Embedded System Design</b>	3	3	0	0	40	60

## Course Objective

This course deals with embedded system designing concepts and developing embedded software with different RTOS and programming languages.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Understand concept of embedded system design and challenges in designing an embedded system
2. Get exposure to designing of memory for embedded applications and interfacing protocols for different peripherals.
3. Understand working with Real time operating systems for embedded software development
4. Get hands on with different programming languages for different type of embedded systems

## Unit 1: Introduction and Examples of Embedded Systems, Concept of Embedded System Design

Design challenge, Processor technology, IC technology, Design technology, Trade-offs. Custom single purpose processor hardware, general-purpose processor: introduction, basic architecture, operation, super-scalar and VLSI architecture, application specific instruction set processors (ASIPs), microcontrollers, digital signal processors, selecting a microprocessor.

## Unit 2: Memory and interfacing modules

Introduction, Memory write ability, Storage performance, Tradeoffs, Common memory types Memory hierarchy and cache AVR 8515 microcontroller: Architecture and Programming in assembly and C. Interfacing Analog and digital blocks: Analog-to-Digital Converters (ADCs), Digital to Analog Converters (DACs), Communication basics and basic protocol concepts, Microprocessor interfacing: I/O addressing, Port and Bus based, I/O, Memory mapped I/O, Standard I/O interrupts, Direct memory access, Advanced communication principles parallel, serial and wireless, Serial protocols I2C, Parallel protocols PCI bus, Wireless protocol IrDA, blue tooth. Different peripheral devices: Buffers and latches, Crystal, Reset circuit, Chip select logic circuit, timers and counters and watch dog timers, Universal asynchronous receiver, transmitter (UART), Pulse width modulators, LCD controllers, Keypad controllers.



## Unit 3: Design Tradeoffs

Design tradeoffs due to thermal considerations and Effects of EMI/ES etc. Software aspect of embedded systems: Challenges and issues in embedded software development, Co-design

## Unit 4: Embedded software development environments

Real time operating systems, Kernel architecture: Hardware, Task/process control subsystem, Device drivers, File subsystem, system calls, Embedded operating systems, Task scheduling in embedded systems: task scheduler, first in first out, shortest job first, round robin, priority based scheduling, Context switch: Task synchronization: mutex, semaphore, Timers.

## Unit 5: Types of embedded operating systems, Programming languages

Assembly languages, high level languages for embedded systems: Embedded system development process Determine the requirements, Design the system architecture, Choose the operating system, Choose the processor, Choose the development platform, Choose programming language, Coding issues, Code optimization, Efficient input/output Testing and debugging, Verify the software on the host system, Verify the software on the embedded system.

## Recommended Books

1. Frankvahid/Tony Givargis, *Embedded System Design- A unified Hardware/software Introduction*.
2. David E Simon, *An embedded software primer*, Pearson education Asia.
3. Dreamteach Software team, *Programming for Embedded System*, AVR 8515 manual
4. J.W. Valvano, *Embedded Microcomputer System: Real Time Interfacing*.
5. Jack Ganssle, *The Art of Designing Embedded Systems*, Newnes.

MTVL-111-18	Credits	L	T	P	Int	Ext
<b>VLSI Design Concepts LAB</b>	2	0	0	4	60	40

## Course Objective

This is one of the fundamental courses meant to give good hands on practice on latest EDA tools in VLSI industry for better understanding the VLSI design issues at circuit level.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Understand the device operation and different technology intricacies in VLSI circuits.
2. Good hands on different tool set of EDA tools (CADENCE, HSPICE) at circuit and layout level.

## Part-A: Experiments

1. NMOS Inverter: Depletion and enhancement mode inverter circuit simulation and modification in circuit parameters.
2. CMOS Inverter: Circuit simulation, adjustment of W / L ratio of P & N channel MOS transistor for symmetrical drive output and loading consideration.
3. Scaling of CMOS Inverter for different technologies, study of secondary effects ( temperature, power supply and process corners).
4. Layout of CMOS Inverter, extraction of parasitics and back annotation and related modifications in circuit parameters and layout.

## Part-B: Lab Projects

Every individual student is required design one Lab Project under the supervision of course teacher. Topic of the project may be any from the theory contents and not limited to following list:

1. Current Source / Mirror: Circuit simulation of current mirror using BJT and MOS ( Simple, Wilson and Widler configurations ) study and modifications to improve power and load regulation. Layout of CMOS current mirror.
2. 8- Bit shift register cell: Building of cell Library of logic gates and flip flops and building of 8 bit shift register from the same. Optimization of the same from layout and power considerations.
3. Differential Amplifier: Study of specifications of differential amplifier and design considerations. Study of input loading and biasing techniques.

MTVL-112-18	Credits	L	T	P	Int	Ext
<b>RTL Simulation &amp; Synthesis with PLD LAB</b>	2	0	0	4	60	40

## Course Objective

This is one of the fundamental courses meant to to give good hands on practice on latest EDA tools in VLSI industry for better understanding of the Digital VLSI design at system level while working with various programmable devices.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Identify, formulate, solve and implement problems in signal processing, communicationsystemsetc using RTL design tools.
2. Use EDA tools like Xilinx, Cadence etc.

## Part-A: Experiments

Verilog implementation of

1. 8:1 Mux/Demux,
2. Full Adder,
3. 8-bit Magnitude comparator,
4. Encoder/decoder,
5. Priority encoder,
6. D-FF,
7. 4-bit Shift registers (SISO, SIPO, PISO, bidirectional),
8. 3-bit Synchronous Counters, Binary to Gray converter,
9. Parity generator.

## Part-B: Lab Projects

Every individual student is required design one Lab Project under the supervision of course teacher. Topic of the project may be any from the theory contents and not limited to following list:

1. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
2. Vending machines - Traffic Light controller, ATM, elevator control.
3. PCI Bus & arbiter and downloading on FPGA.
4. UART/ USART implementation in Verilog.
5. Realization of single port SRAM in Verilog.
6. Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
7. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.



MTRM-101-18	Credits	L	T	P	Int	Ext
<b>Research Methodology and IPR</b>	2	2	0	0	40	60

## Course Objective

This is one of the fundamental courses which help post graduate students to better conduct their research problem in a systematic way and helps in how to take forward the research for communication.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Understand research problem formulation.
2. Analyze research related information and follow research ethics
3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

## Unit 1: Research Problem

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

## Unit 2: Effective literature studies approaches

Effective literature studies approaches, analysis Plagiarism, Research ethics

## Unit 3: Effective technical writing

Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

## Unit 4: Nature of Intellectual Property

Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

## Unit 5: Patent Rights

Scope of Patent Rights.Licensing and transfer of technology.Patent information and databases.Geographical Indications.

## Unit 6: Developments in IPR

Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and



## Recommended Books

1. Stuart Melville and Wayne Goddard, *Research methodology: an introduction for science & engineering students*.
2. Wayne Goddard and Stuart Melville, *Research Methodology: An Introduction*.
3. Ranjit Kumar, 2nd Edition, *Research Methodology: A Step by Step Guide for beginners*.
4. Halbert, *Resisting Intellectual Property*, Taylor & Francis Ltd, 2007.
5. Mayall, *Industrial Design*, McGraw Hill.
6. Niebel, *Product Design*, McGraw Hill.
7. Asimov, *Introduction to Design*, Prentice Hall.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, *Intellectual Property in New Technological Age*.
9. T. Ramappa, *Intellectual Property Rights Under WT*, S. Chand



# SECOND SEMESTER

## M.Tech (VLSI Design)

MTVL-103-18	Credits	L	T	P	Int	Ext
Analog, Digital & Mixed Signal CMOS Design	3	3	0	0	40	60

### Course Objective

This is one of the basic VLSI course meant to give an overview of various CMOS based analog, digital and mixed signal logic circuits

### Course Outcomes

At the end of this course student will demonstrate the ability to:



1. Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
2. Connect the individual gates to form the building blocks of a system.
3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools likeNgspice.

## Unit 1: Review

Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power.

## Unit 2: Physical design flow

Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

## Unit 3: Sequential logic

Static latches and registers, Bi-stability principle, MUX based latches,Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High-k, Metal Gate Technology, FinFET, TFET etc.

## Unit 4:Single Stage Amplifier

CS stage with resistance load, Divide connected load, Currentsource load, Triode load, CS stage with source degeneration, Source follower, Common gatestage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

## Unit 5: Passive and active current mirrors

Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise.

## Unit 6: Operational amplifiers

One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

## Recommended Books

1. J P Rabaey, A P Chandrakasan, B Nikolic, *Digital Integrated circuits: A design perspective*, Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, *CMOS Circuit Design, Layout, and Simulation*, Wiley, 2nd Edition.
3. BehzadRazavi, *Design of Analog CMOS Integrated Circuits*, TMH, 2007.
4. Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*, Oxford, 3<sup>rd</sup>Edition.
5. R J Baker, *CMOS circuit Design, Layout and Simulation*, IEEE Inc., 2008.
6. Kang, S. and Leblebici, Y., *CMOS Digital Integrated Circuits, Analysis and Design*, TMH, 3rdEdition.
7. Pucknell, D.A. and Eshraghian, K., *Basic VLSI Design*, PHI, 3rd Edition.



MTVL-104-18	Credits	L	T	P	Int	Ext
<b>VLSI Design Verification &amp; Testing</b>	3	3	0	0	40	60

## Course Objective

This is one of the fundamental VLSI courses meant to give a brief overview of verification and testing guidelines for digital circuits.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Familiarity of Front end design and verification techniques and create reusable test environments.
2. Will get exposure to testing methodologies and ATPG algorithms for combinational and Sequential circuits.
3. Use EDA tools like Cadence.

## Unit 1: Introduction

Introduction to testing, VLSI trends affecting testing,

## Unit 2: Verification guidelines

Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

## Unit 3: Data types

Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

## Unit 4: Faults in Digital Circuits

Physical Faults, Stuck-at Faults, Stuck open Faults, Permanent, Intermittent and Pattern Sensitive Faults, Delay Faults, Modeling of faults, Logical Fault Models, Fault Equivalence, Fault dominance

## Unit 5: Design Verification

Modeling Levels and Types of Simulators, True value simulation algorithm - Compiled-Code, Event-Driven; Fault Simulation algorithm- Serial, Parallel, Deductive and Concurrent Fault Simulation. Path Sensitization Methods, Roth's D- Algorithm, PODEM Algorithm, Complexity of Sequential ATPG.

## Unit 6: Design for Testability

Ad-hoc design, generic scan based design, classical scan based design, system level DFT approaches, Built-In self-test, test pattern generation for BIST, Circular BIST, BIST Architectures, Testable Memory Design, Test Algorithms, Boundary Scan Standard - TAP Controller, Test Instructions.

## Recommended Books

1. Chris Spears, *System Verilog for Verification*, Springer, 2nd Edition

2. M. Bushnell and V. D. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Kluwer Academic Publishers
3. IEEE 1800-2009 standard (IEEE Standard for System Verilog- Unified Hardware Design, Specification, and Verification Language).
4. General reuse information and resources [www.design-reuse.com](http://www.design-reuse.com)
5. OVM, UVM(on top of SV) [www.verificationacademy.com](http://www.verificationacademy.com)

MTVL-PE3A-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 3</b> <b>Low Power VLSI Design</b>	3	3	0	0	40	60

## Course Objective

This course deals with low power design methods for various high performance and reliable VLSI Design varying from circuit to system level.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
2. Characterize and model power consumption & understand the basic analysis methods.
3. Understand leakage sources and reduction techniques.

## Unit 1: Technology & Circuit Design Levels

Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of  $V_{dd}$  &  $V_t$  on speed, constraints on  $V_t$  reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

## Unit 2: Low Power Circuit Techniques

Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

## Unit 3: Low Power Clock Distribution

Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network.

## Unit 4: Logic Synthesis for Low Power estimation techniques

Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

## Unit 5: Low Power Memory Design

Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

## Unit 6: Low Power Microprocessor Design System

Power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

## Recommended Books

1. P. Rashinkar, Paterson and L. Singh, *Low Power Design Methodologies*, Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, *Low power CMOS VLSI circuit design*, John Wiley sons Inc., 2000.
3. J.B.Kulo and J.H Lou, *Low voltage CMOS VLSI Circuits*, Wiley, 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, *Low power digital CMOS design*, Kluwer, 1995
5. Gary Yeap, *Practical low power digital VLSI design*, Kluwer, 1998.

MTVL-PE3B-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 3 Modeling and Simulation</b>	3	3	0	0	40	60

## Course Objective

This is course deals with various Modeling and Simulation schemes and their issues for components in an IC

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Understand different modeling and timing issues for components in an IC
2. Understand extraction of statistical behavior of data and methods to find Probability
3. Understand various modeling schemes for simulation

## Unit 1: Component model for ICs

Design rule checks, timing verification worst case delay simulation, setup and hold times for clocked devices; Behaviour modeling, structural modeling, simulation with the physical model; Hardware Description Language.

## Unit 2: Statistical

Description of data, Data-fitting methods, Regression analysis, Analysis of Variance, Goodness of fit.

## Unit 3: Probability and Random Processes

Discrete and Continuous Distribution, Central Limit theorem, Measure of Randomness, Monte Carlo Methods.

## Unit 4: Stochastic Processes



Stochastic Processes and Markov Chains, Time Series Models.

## Unit 5: Modelling and simulation

Concepts, Discrete-event simulation: Event scheduling/Time advance algorithms, Verification and validation of simulation models.

## Unit 6: Continuous simulation

Modelling with differential equations, Example models, Bond Graph Modelling, Population Dynamics Modelling, System dynamics.

## Recommended Books

1. James R., Armstrong J.R., *Chip-level Modelling with VHDL*, Prentice Hall
2. Navalih, Z., VHDL, *Analysis and Modelling of Digital Systems*
3. Banks J, Carson JS and Nelson B, *discrete-Event System simulation*, 2nd Edition, Prentice-Hall of India
4. Winston, W.L., *Operations Research : applications and algorithms*, 3rd Edition, Duxbury press, Belmont, California

MTVL-PE3C-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 3</b> <b>Nano Materials &amp; Nano Technology</b>	3	3	0	0	40	60

## Course Objective

This is course deals with fundamental behavior of Nano Materials and competing nano technologies for various applications

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. To understand the basic science behind the design and fabrication of nano scale systems.
2. To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
3. To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
4. To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

## Unit 1: Nanomaterials in one and higher dimensions,

Types of Nano-Materials, Special Magnetic Nanomaterials, Quantum mechanical Properties, Nanomaterials in dimensions.

## Unit 2: Applications of one and higher dimension nano-materials

Applications of one and higher dimension nano-materials, Magneto Resistance effects in magnetic materials, Spin Valve Effect, Medical Nanomaterials.



## Unit 3: Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics

Lithography, Some Tools of Micro Nano Fabrication micro electro-mechanical system (MEMS) and nano-phonics: Optical Nano materials  
Excitons, band-gap variations-quantum confinement (quantum dots)

## Unit 4: Unit 4: carbon nanotubes – synthesis and applications

Carbon nanotubes – synthesis, Functionalization and applications: CNT-FET, Memories

## Unit 5: Interdisciplinary arena of nanotechnology-I

Nano Physics & Nano Electronics: SET, FinFET, Quantum computers, Optical Nanomaterials

## Unit 6: Interdisciplinary arena of nanotechnology-II

Nano Chemistry: Nanoparticles, bonds in nanomaterials, Nano Biology & Nano Medicine: Bio-Nanomaterials, Drug delivery

## Recommended Books

1. Kenneth J. Klabunde and Ryan M. Richards, *Nanoscale Materials in Chemistry*, 2<sup>nd</sup>edn, John Wiley and Sons.
2. A I Gusev and AARempel, *Nanocrystalline Materials*, Cambridge International Science Publishing.
3. Bharat Bhushan, *Springer Handbook of Nanotechnology*, Springer, 3<sup>rd</sup>edn.
4. Kamal K. Kar, Research, *Carbon Nanotubes: Synthesis, Characterization and Applications*.

MTVL-PE4A-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 4</b> <b>Semiconductor Devices Physics</b>	3	3	0	0	40	60

## Course Objective

This is course deals with fundamental concepts of Semiconductor Physics for modeling of various Semiconductor Devices and emerging Nano- Devices

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Fundamentals of quantum mechanics, transport phenomenon in semiconductor followed by two junctions three junction devices.
2. Study of energy band diagrams and equivalent models will help to understand the physics in ideal and non-ideal conditions.

## Unit 1: Semiconductor Physics Fundamentals



Quantum Mechanics Concepts, Schrodinger wave equation, Carrier Concentration, Drift Velocity, Diffusion Transport Equation, Mobility effects, Hall Effect, Continuity Equation, Carrier Generation and Recombination, Shockley Read Hall Theory of Recombination.

## Unit 2: PN Junction

PN Junction: Energy band diagrams, Step junction, linearly graded junction, I-V Characteristics, Junction break down Phenomenon- Zener, Avalanche Process.

## Unit 3: Bipolar Junction Transistor

Introduction to BJT, Transistor Action, Minority carrier distribution profile, Equivalent Models -Ebers - Molls Model, Gummel Poon Model, Non-ideal effects in BJT- Early effect, High Injection etc.

## Unit 4: MOSFET Modeling

Introduction Interior Layer, MOS Transistor Current, Energy band diagram, Threshold Voltage, Work function difference, Flat band voltage, Depletion layer thickness, Charge distribution, C-V characteristics, I-V Characteristics.

## Unit 5: Non-ideal Effects in MOSFET

Short Channel and Narrow Width Effect, Sub-threshold Conduction, Channel length modulation, Velocity saturation,  $V_T$  roll-off, Drain Induced Barrier Lowering, Gate Induced Drain Leakage, Gate Tunneling, Punch through.

## Unit 6: Emerging Nano- Devices

Introduction to Nano-devices and structures, Transport Phenomenon.

## Recommended Books

1. Donald A. Neamen, *Semiconductor Physics and Devices*, 3rd Edition, McGraw Hill.
2. Ben G. Streetman, Sanjay Banerjee, *Solid state electronic devices*, Pearson Education, 7th Edition.
3. Edward S. Yang, *Fundamentals of Semiconductor Devices*, Mc-Graw Hill.
4. S.M. Sze, *Physics of Semiconductor Devices*, Wiley Eastern.
5. Tsividis, Yannis, *Operation and modeling of the MOS transistor*, Oxford University Press, 2nd Edition.
6. Pail Richman, *MOS Field Effect Transistor and Integrated Circuits*, John Wiley and Sons.

MTVL-PE4B-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 4 Parallel Processing</b>	3	3	0	0	40	60

## Course Objective

This is course deals with fundamental concepts of Parallel Processing and Parallel Programming techniques for various high-performance processor architectures.

## Course Outcomes

At the end of this course student will demonstrate the ability to:



1. Identify limitations of different architectures of computer and significance of parallel processing and pipelining for better performance
2. Understand and critical review various parallel processor architectures: VLIW, Superscalar etc
3. Understand the details of performance enhancement Parallel Programming Techniques and Multithreading

## Unit 1: Parallel Processing

### Unit 1: Introduction

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability.

### Unit 2: Pipelining

Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.

### Unit 3: Case study

VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.

### Unit 4: Multithreading

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

### Unit 5: Parallel Programming Techniques

Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues.

### Unit 6: Applications

Operating systems for multiprocessors systems, Customizing applications on parallel processing platforms.

## Recommended Books

1. Kai Hwang, Faye A. Briggs, *Computer Architecture and Parallel Processing*, MGH International Edition
2. Kai Hwang, *Advanced Computer Architecture*, TMH
3. V.Rajaraman, L. Sivaram Murthy, *Parallel Computers*, PHI.
4. William Stallings, *Computer Organization and Architecture, Designing for performance*, Prentice Hall, Sixth edition
5. Kai Hwang, Zhiwei Xu, *Scalable Parallel Computing*, MGH.
6. David Harris and Sarah Harris, *Digital Design and Computer Architecture*, Morgan Kaufmann.

MTVL-PE4C-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 4 System on Chip (SOC)</b>	3	3	0	0	40	60

## Course Objective



This course deals with fundamental concepts of system-on-chip approach of designing complex VLSI systems and challenges.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Identify and formulate a given problem in the framework of SoC based design approaches.
2. Design SoC based system for engineering applications.
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development

## Unit 1: ASIC

ASIC - Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts

## Unit 2: NISC

NISC- NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for Specification, compilation and synthesis of embedded processors.

## Unit 3: Simulation

Simulation - Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

## Unit 4: Low power SoC design / Digital system

Low power SoC design / Digital system, - Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

## Unit 5: Synthesis

Synthesis- Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.

## Unit 6: Case Study

Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

## Recommended Books

1. Hubert Kaeslin, *Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication*, Cambridge University Press.
2. B. Al Hashimi, *System on chip-Next generation electronics*, The IET.
3. Rochit Rajsuman, *System-on-a-chip: Design and test*, Advantest America R & D Center.
4. P Mishra and N Dutt, *Processor Description Languages*, Morgan Kaufmann.

5. Michael J. Flynn and Wayne Luk, *Computer System Design: System-on-Chip*, Wiley.

MTVL-113-18	Credits	L	T	P	Int	Ext
Analog, Digital & Mixed Signal CMOS Design LAB	2	0	0	4	60	40

## Course Objective

This course provides good hands on practice of latest EDA tools to understand and to design various analog/digital CMOS based circuits.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Design digital and analog Circuit using CMOS.
2. Use EDA tools like Cadence, Mentor Graphics and other open source software tools

## Part-A: Experiments

1. Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
  - a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
  - b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
  - c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
  - d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
  - e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV.
    - i. To extract Vth use the following procedure.
  - f) Plot gm vs VGS using NGSPICE and obtain peak gm point.
  - g) Plot  $y=ID/(gm)^{1/2}$  as a function of VGS using Ngspice.
  - h) Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
  - i) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.
    - i. Tabulate your result according to technologies and comment on it.
2. Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
  - a) Perform the following
    - i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
    - ii. Plot VTC for CMOS inverter with varying VDD.
    - iii. Plot VTC for CMOS inverter with varying device ratio.
  - b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Clod = 50fF)
  - c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Clod = 4pF, Rload = k).
3. Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4. Perform the following
  - i. Draw small signal voltage gain of the minimum-size inverter in 0.18 $\mu$ m and 0.13 $\mu$ m technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18 $\mu$ m and 0.13 $\mu$ m process.
  - ii. Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18 $\mu$ m technology.  $(W/L)_{MN}=5$ ,  $(W/L)_{MP}=10$  and  $L=0.5\mu$ m for both transistors.
  - iii. Establish a test bench, as explained in the lecture, to achieve  $V_{DSQ}=V_{DD}/2$ .
  - iv. Calculate input bias voltage if bias current=50 $\mu$ A.
  - v. Use Ngspice and obtain the bias current. Compare its value with 50 $\mu$ A.
  - vi. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).
  - vii. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
  - viii. Use Ngspice to determine input voltage range of the amplifier

## Part-B: Lab Projects

Every individual student is required design one Lab Project under the supervision of course teacher. Topic of the project may be any from the theory contents and not limited to following list:

1. Three OPAMP INA.  $V_{dd}=1.8V$   $V_{ss}=0V$ , CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10.
2. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
  - i. Draw the schematic of op-amp macro model.
  - ii. Draw the schematic of INA.
  - iii. Obtain parameters of the op-amp macro model such that
    - a. low-frequency voltage gain =  $5 \times 10^4$ ,
    - b. unity gain BW ( $f_u$ ) = 500KHz,
    - c. input capacitance=0.2pF,
    - d. output resistance
    - e. CMRR=120dB
  - iv. Draw schematic diagram of CMRR simulation setup.
  - v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
  - vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
  - vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.
3. Technology: UMC 0.18 $\mu$ m,  $V_{DD}=1.8V$ . Use MAGIC or Microwind.
  - i. Draw layout of a minimum size inverter in UMC 0.18 $\mu$ m technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
  - ii. Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
  - iii. Use extracted netlist and obtain  $t_{PHL}$  and  $t_{PLH}$  for the middle inverter using Eldo.
  - iv. Use interconnect length obtained and connect the second and third inverter.
4. Extract the new netlist and obtain  $t_{PHL}$  and  $t_{PLH}$  of the middle inverter. Compare new
  - i. values of delay times with corresponding values obtained in part 'c'.



MTVL-114-18	Credits	L	T	P	Int	Ext
<b>VLSI Design Verification &amp; Testing LAB</b>	2	0	0	4	60	40

## Course Objective

This course provides good hands on practice of latest EDA tools to understand and to design, implement and test various digital VLSI designs.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Verify increasingly complex designs more efficiently and effectively.
2. Use EDA tools like Cadence, Mentor Graphics.

## Experiments

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions



# THIRD SEMESTER

## M.Tech (VLSI Design)

MTVL-PE5A-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 5</b> Sensor Technology and MEMS	3	3	0	0	40	60



## Course Objective

This course deals with design and modeling of various sensors with MEMS and gives an overview of Micromachining techniques used for MEMS development

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Understand the concept of MEMS and their fabrication techniques review along with different sensors overview
2. Get an overview of Micromachining techniques used for MEMS development
3. Understand the modeling of smart sensors

## Unit 1: Introduction

Historical Development of Microelectronics, Evolution of Micro sensors, Evolution of MEMS, Emergence of Micro machines, Sensor Systems, Sensors types and classification, Mechanical Sensors, Acoustic Sensors, Magnetic Sensors, Thermal Sensors, Optical sensors Chemical Sensors, Radiation Sensors and Biosensors. Micro sensors, Sensors based on surface-acoustic wave devices. Review Of Fabrication Techniques (Lithography, PVD,CVD,RIE)

## Unit 2: Micromachining techniques

Introduction to Bulk Micromachining, Isotropic and Orientation-Dependent Wet Etching, Dry Etching, Buried Oxide Process, Silicon Fusion Bonding, Sacrificial Layer Technology, Surface Micromachining using Plasma Etching, Combined IC Technology and Anisotropic Wet Etching, Processes Using Both Bulk and Surface Micromachining, Adhesion Problems in Surface Micromachining, Surface Versus Bulk Micromachining.

## Unit 3: Smart Sensors and Modeling

Introduction to Smart Sensors, Integrated Smart sensors and smart systems, MEMS and NEMS devices, Elastic structures in MEMS and NEMS, Modeling of Thermal Elastic systems, Electrostatic-elastic systems, magnetically actuated systems, Microfluidics (Membrane Pumps, Nanolithography, Nano jets)

## Recommended Books

1. John A. Pelesko and David H. Bernstein, *Modeling MEMS and NEMS*, Chapman & Hall/CRC
2. Vikas Choudhary and Krzysztof Iniewski, *MEMS Fundamental Technology and Applications*, CRC press
3. Julian W. Gardner, Vijay K. Varadan, *Micro sensors, MEMS and Smart devices*, John Wiley & Sons, Ltd
4. C.M. Meijer, *Smart Sensor Systems* Gerard, John Wiley & Sons, Ltd.
5. Ristic L (ed), *Sensor Technology and Devices*, Artech House, London.
6. Sze S.M. (ed), *Semiconductor Sensors*, John Wiley, New York.
7. K.D. (Guest Editor), *Integrated Sensors, Microp-actuators and micro-systems MEMS*, Special Issue of proceedings of IEEE, Vol. 86, No.8, August 1998.

MTVL-PE5B-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 5</b>	3	3	0	0	40	60



## Course Objective

This course deals with the challenges in Device Characterization process which faces increasing challenges in electrical test for more and more sophisticated devices due to emergence of the new device technologies, new materials, processes development and integration,

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Perform electrical on-wafer measurements of devices (Device Characterization) with various methods
2. Understand Generation-recombination statistics, Optical measurements for Recombination lifetime
3. Get introduced to Thin Film Thickness-Measurements

## Unit 1: Resistivity

Wafer mapping, two point versus four point probe, resistivity profiling (differential hall effect, spreading resistance profiling), contactless methods. Carrier Doping: Capacitance-voltage(C-V), current-voltage(I-V), optical techniques. Contact resistance and Schottky Barriers: metal-semiconductor contacts, measurement techniques, schottky barrier height.

## Unit 2: Defects

Generation-recombination statistics, deep-level transient Spectroscopy (DLTS), Carrier life time: recombination lifetime/surface recombination velocity, generation lifetime/surface generation velocity.

## Unit 3: Recombination lifetime

Optical measurements : photo conductance decay, quasi-steady state photo conductance, free carrier absorption, electron beam induced current, short circuit current/open circuit voltage decay. Recombination lifetime-electrical measurements: diode current-voltage, reverse recovery, open circuit voltage decay, pulsed MOS capacitor. Generation lifetime-Electrical measurements: gatecontrolled diode, pulsed MOS Capacitor. Physical Characterization.

## Unit 4: Thin Film Thickness-Measurements

Ellipsometry, surface profiling, spectrophotometry, FTIR Critical Dimension Measurements: Optical microscope, Scanning Electron Microscope, Transmission Electron Microscope Material and Impurity Characterization: SIMS, XRD, EDAX Electrical Characterization:, sheet resistance C-V measurements, DLTS, Carrier lifetime, impurity profiling, I-V measurements, Process and SPICE model parameter Extraction.

## Recommended Books

1. W.R. Reunyan, *Semiconductor Measurements and Instrumentation*, Mc-Graw Hill, 2nd Edition.
2. Schroder, *Semiconductor Material And Device Characterization*, 2nd edition, Wiley-Interscience, 2nd edition.

3. Philips F. Kare and Greydon B. Lauabee, *Characterization of semiconductor Materials*, McGraw Hill, 2nd edition.
4. K.V. Ravi, *Imperfections and Impurities In Semiconductor Silicon*, John Wiley & Sons Inc., 1st edition.
5. Tor A. Fjeldly, TrondYtterdal, Michael Shur ,*Introduction to device modeling and circuit simulation* ,Wiley, 3rd edition.
6. By JianjunGao ,*Optoelectronic Integrated Circuit Design and Device Modeling*, Wiley.

MTVL-PE5C-18	Credits	L	T	P	Int	Ext
<b>Program Elective – 5</b> <b>RF Circuit Design</b>	3	3	0	0	40	60

## Course Objective

This is course deals with design issues in RF and Wireless Technology for power efficient RF Communication systems and how to implement them in VLSI.

## Course Outcomes

At the end of this course student will demonstrate the ability to:

1. Understand RF and Wireless Technology issues and how to choose between them for an application based on various performance parameters.
2. Understand power efficiency techniques for high speed Mobile RF Communication systems
3. Explore different Receiver and Transmitter Architectures at RF frequencies and their VLSI implementation
4. Different Power amplifiers and Oscillators at RF frequencies
- 5.

## Unit 1: Introduction

Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology. Basic concepts in RF Design: Nonlinearly and Time Variance, intersymbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.

## Unit 2: Analog and Digital Modulation for RF circuits

Comparison of various techniques for power efficiency.Coherent and Non coherent deflection.Mobile RF Communication systems and basics of Multiple Access techniques.

## Unit 3: Receiver and Transmitter Architectures

Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters.BJT and MOSFET behaviour at RF frequencies modelling of the transistors and SPICE models.Noise performance and limitation of devices.Integrated parasitic elements athigh frequencies and their monolithic implementation.

## Unit 4: Basic blocks in RF systems





Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations.

## Unit 5: Oscillators

Basic topologies VCO and definition of phase noise.Noise-Power trade-off.Resonator less VCO design. Quadrature and single-sideband generators, Radio FrequencySynthesizes: PLLS, Various RF synthesizer architectures and frequency dividers.

## Unit 6: Power Amplifiers design

Power Amplifiers design. Linearization techniques, Design issues in integrated RF filters, Somediscussion on available CAD tools for RF VLSI designs

## Recommended Books

1. John A. Pelesko and David H. Bernstein ,*Modeling MEMS and NEMS* , Chapman & Hall/CRC
2. B.Razavi, *RF Microelectronics*, Prentice-Hall PTR.
3. T.H.Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Press.
4. R.JacobBaker,H.W.Li, and D.E. Boyce, *CMOS Circuit Design ,Layout and Simulation*, Prentice-Hall of .
5. Y.P. Tsividis,*Mixed Analog and Digital VLSI Devices and Technology*, McGraw Hill.

## MTAC-AXX-18 Audit Courses -1

MTAC-AO1-18	Credits	L	T	P	Int	Ext
English for research paper writing	0	2	0	0	40	60

## Course Objective

This course is to develop skills in effective English writing to communicate the research work

## Course Outcomes

At the end of this course Students will be able to:

1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title
4. Ensure the good quality of paper at very first-time submission

## Unit 1



Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

## Unit 2

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction

## Unit 3

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

## Unit 4

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

## Unit 5

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

## Unit 6

Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

## Recommended Books :

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

MTAC-A02-18	Credits	L	T	P	Int	Ext
<b>Disaster Management</b>	0	2	0	0	40	60

## Course Objective

This course is to develop skills in helping society during natural disasters and how to manage.

## Course Outcomes

At the end of this course students will be able to:

1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in

## Unit 1

Introduction: Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.

## Unit 2

Repercussions Of Disasters And Hazards: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

## Unit 3

Disaster Prone Areas In India Study Of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics.

## Unit 4

Disaster Preparedness And Management Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

## Unit 5

Risk Assessment Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.

## Unit 6

Disaster Mitigation Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.

## Recommended Books :

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies" New Royal book Company.
2. Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep & Deep Publication Pvt. Ltd., New Delhi.

MTAC-A03-18	Credits	L	T	P	Int	Ext
<b>Sanskrit For Technical Knowledge</b>	0	2	0	0	40	60

## Course Objective

This course is to develop

1. A working knowledge in illustrious Sanskrit, the scientific language in the world
2. Learning of Sanskrit to improve brain functioning

3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power
4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature

## Course Outcomes

At the end of this course students will be able to

1. Understanding basic Sanskrit language
2. Ancient Sanskrit literature about science & technology can be understood
3. Being a logical language will help to develop logic in students

## Unit 1

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences.

## Unit 2

Order, Introduction of roots, Technical information about Sanskrit Literature.

## Unit 3

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

## Recommended Books :

1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

MTAC-A04-18	Credits	L	T	P	Int	Ext
Value Education	0	2	0	0	40	60

## Course Objective

This course is to develop

1. Value of education and self- development
2. Imbibe good values in students
3. Let the should know about the importance of character

## Course Outcomes

At the end of this course students will be able to

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

## Unit 1

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism, Moral and non- moral valuation. Standards and principles, Value judgements.

## Unit 2

Importance of cultivation of values, Sense of duty, Devotion, Self-reliance, Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity, Power of faith, National Unity, Patriotism, Love for nature, Discipline.

## Unit 3

Personality and Behavior Development - Soul and Scientific attitude, Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour, Universal brotherhood and religious tolerance, True friendship, Happiness Vs suffering, love for truth, Aware of self-destructive habits, Association and Cooperation, Doing best for saving nature.

## Unit 4

Character and Competence –Holy books vs Blind faith, Self-management and Good health, Science of reincarnation, Equality, Nonviolence, Humility, Role of Women, All religions and same message, Mind your Mind, Self-control, Honesty, Studying effectively.

## Recommended Books :

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi

## MTAC-AXX-18 Audit Courses -2

MTAC-A05-18	Credits	L	T	P	Int	Ext
<b>Constitution of India</b>	0	2	0	0	40	60

## Course Objective

This course is to

1. Understand the premises informing the twin themes of liberty and freedom from a civilrights perspective.
2. To address the growth of Indian opinion regarding modern Indian intellectuals’ constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

## Course Outcomes

Students will be able to:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.



3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

## Unit 1:

History of Making of the Indian Constitution:History, Drafting Committee, (Composition & Working).

## Unit 2:

Philosophy of the Indian Constitution:Preamble, Salient Features.

## Unit 3:

Contours of Constitutional Rights &Duties:Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State PolicyFundamental Duties.

## Unit 4:

Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

## Unit 5:

Local Administration: District's Administration head: Role and Importance,Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation, Pachayati raj: Introduction, PRI: ZilaPachayat, Elected officials and their roles, CEO ZilaPachayat: Position and role, Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials,Importance of grass root democracy.

## Unit 6:

Election Commission:Election Commission: Role and Functioning, Chief Election, Commissioner and Election Commissioners, State Election Commission: Role and Functioning,Institute and Bodies for the welfare of SC/ST/OBC and women.

## Recommended Books :

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

MTAC-A06-18	Credits	L	T	P	Int	Ext
<b>Pedagogy Studies</b>	0	2	0	0	40	60

## Course Objective

This course is to inculcate better teaching methods/tools for future teachers to build a better education system to compete with the developed nations pedagogical practices

## Course Outcomes

Students will be able to understand:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

### Unit 1:

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education, Conceptual framework, Research questions, Overview of methodology and Searching.

### Unit 2:

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries, Curriculum, Teacher education.

### Unit 3:

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included, studies, How can teacher education (curriculum and practicum) and the school, curriculum and guidance materials best support effective pedagogy? Theory of change, Strength and nature of the body of evidence foreffective pedagogical practices, Pedagogic theory and pedagogical approaches, Teachers' attitudes and beliefs and Pedagogic strategies.

### Unit 4:

Professional development: alignment with classroom practices and follow-up support Peer support, Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

### Unit 5:

Research gaps and future directions- Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

## Recommended Books :

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272-282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. [www.pratham.org/images/resource%20working%20paper%202.pdf](http://www.pratham.org/images/resource%20working%20paper%202.pdf)



MTAC-A07-18	Credits	L	T	P	Int	Ext
<b>Stress Management By Yoga</b>	0	2	0	0	40	60

## Course Objective

This course helps to achieve overall health of body and mind and overcome stress

## Course Outcomes

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

### Unit 1:

Definitions of Eight parts of yog. ( Ashtanga )

### Unit 2:

Yam and Niyam, Do's and Don't's in life. i) Ahinsa, satya, astheya, bramhacharya and aparigraha, ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan.

### Unit 3:

Asan and Pranayam, i) Various yog poses and their benefits for mind & body ii) Regularization of breathing techniques and its effects-Types of pranayam.

### Recommended Books :

1. 'Yogic Asanas for Group Training-Part-I' : Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama(Publication Department), Kolkata

MTAC-A08-18	Credits	L	T	P	Int	Ext
<b>Personality Development Through Life Enlightenment Skills</b>	0	2	0	0	40	60

## Course Objective

This course helps to learn to achieve the highest goal happily, become a person with stable mind, pleasing personality and determination and awaken wisdom in students

## Course Outcomes

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students.





## Unit 1:

Neetisatakam-Holistic development of personality, Verses- 19,20,21,22 (wisdom), Verses- 29,31,32 (pride & heroism), Verses- 26,28,63,65 (virtue), Verses- 52,53,59 (dont's), Verses- 71,73,75,78 (do's).

1

## Unit 2:

Approach to day to day work and duties, Shrimad BhagwadGeeta : Chapter 2-Verses 41, 47,48, Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35, Chapter 18-Verses 45, 46, 48.

## Unit 3:

Statements of basic knowledge, Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 Chapter 12 - Verses 13, 14, 15, 16,17, 18, Personality of Role model. Shrimad Bhagwad Geeta: Chapter2-Verses 17, Chapter 3-Verses 36,37,42, Chapter 4-Verses 18, 38,39, Chapter18 – Verses 37,38,63.

## Recommended Books :

1. "Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, RashtriyaSanskritSansthanam, New Delhi.